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System,Plant Level, Enterprise level

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Given the overwhelming success of

DeviceNet, it's not surprising that ODVA and Rockwell Automation would be interested in pursuing technology solutions for implementing Industrial Ethernet at the ...

Ethernet at the Device-Level

Texas Instruments (TI) (Nasdaq: TXN)

today introduced a new high-performance microcontroller (MCU) portfolio that advances real-time ...

New MCU portfolio redefines microcontroller performance, enabling 10 times higher processing capability than existing devices

Zebra Technologies announces its intention to purchase Fetch Robotics. Two leaders within industrial environments are joining forces as Zebra Technologies announced its intention to acquire Fetch ...

Zebra Fetches Automation Integration

Applitools, provider of next generation

test automation platform through Visual AI and Ultrafast Test Cloud, today announced the ...

Applitools Unveils Innovative New Approach for Native Mobile Test Automation

The everlasting rat□s nest that is scientific

computing data management, the permanent quest for more advanced-level processing power, and investments in new fabs for advanced chips are HPC topics in ...

HPC in the News: Data Management Automation and Faster Processor Gates;

Intel and TSMC in Arizona, Europe

The latest Allen-Bradley PanelView Plus 7 Performance graphic terminal expands on the recently released standard model, boasting a larger screen size, faster processor, software support and expanded ...

Rockwell Automation updates graphic terminal range

Growing data, new technology, and data-driven decisions fuel big data & analytics. Discover & explore this year's big data trends now.

Big Data Trends in 2021 and The Future

of Big Data

It's important for people who implement AI and related projects to strike the right balance between cost pressure and revenue pressure, efficiencies and insights and hyperautomation and ...

Balancing Hyperautomation And

Hyperpersonalization

Medical Product Outsourcing published an article about medtech and micromolding that made me think about the future of micro 3DP for medical devices. Smarter, faster, cheaper. Those three words have ...

Smaller, faster, cheaper: The future of

medical device manufacturing

As IoT continues to influence the engineering industry, Bosch Rexroth in a recent white paper listed the five key factors of product design ... and devices into existing automation structures.

5 Key Factors for IoT Devices

What are we doing to ensure we don't make the same mistakes again? Follow along for my breakdown below. The office and the technology you implement must drive purpose for employees to come into the ...

How to Stop Making the Same Mistakes

Over and Over Again

Inc. (Nasdaq: ADI) has expanded its ADI Chronous Industrial Ethernet portfolio with solutions that bring long-reach Ethernet connectivity from the edge to the cloud and enable real-time ...

Analog Devices Announces Long-Reach

Industrial Ethernet Offerings to Achieve Last Mile Connectivity in Process, Factory and Building Automation

That's actually what my team and I have been increasingly hearing from automotive brands and parts manufacturers lately. With the economy starting to recover and production still slightly depressed, ...

Machine Vision Systems Deserve a Second Look by Auto Manufacturers Right Now. This is Why.

In addition, key acquisitions of Plex Systems and Fiix have boosted and expanded its offerings to help companies bring IT and operational technology (OT)

together. We see a growing need to improve ...

Plex, Fiix acquisitions bridging IT and OT
Vibration Level Switch Market Snapshot
Vibration level switches have numerous benefits including ease of installation the ability to setup and commission without

the need of a medium is anticipated to ...

Vibration Level Switch Market May See a Big Move: Growth Size, Major Giants Future Share and Forecast 2028

Soloinsight, the security workflow automation platform company, will showcase its CloudGate SmartSpace

solution during ISC West at booth #9100. ISC West is held at the Sands Convention Centre in ...

Soloinsight to showcase their CloudGate SmartSpace solution at ISC West 2021 Market Overview: According to a comprehensive research report by

(MRFR), "Global Field Force Automation Market information by Deployment, by Components, by Organization Size and Region – forecast to ...

Field Force Automation Market to Reach USD 3.05 Billion by 2025 at 15.2% CAGR - Report by Market Research

Future (MRFR)

The ever-increasing demand for factory-level data by higher level systems ... TSN will ensure time-critical data like automation traffic gets to where it needs to go on the network while maintaining ...

10 ways time-sensitive networking will

change industrial automation

This model includes a second circuit board level for customization with a variety of optional interfaces or an integrated 1-sec. UPS. It is designed as a modular automation device with an ...

Industrial PC Offers Edge, Computing

Power

This ensures a higher level ... test automation use cases -- Functional Testing, Visual Testing, Web and Mobile UI/UX Testing, Cross Browser Testing, Responsive Web Design Testing, Cross Device ...

This book presents a detailed summary of research on automatic layout of device-level analog circuits that was undertaken in the late 1980s and early 1990s at Carnegie Mellon University. We focus on the work behind the creation of the tools

called KOAN and ANAGRAM II, which form part of the core of the CMU ACACIA analog CAD system. KOAN is a device placer for custom analog cells; ANANGRAM II a detailed area router for these analog cells. We strive to present the motivations behind the architecture of these tools, including detailed discussion

of the subtle technology and circuit concerns that must be addressed in any successful analog or mixed-signal layout tool. Our approach in organizing the chapters of the book has been to present our algo rithms as a series of responses to these very real and very difficult analog layout problems. Finally, we present

numerous examples of results generated by our algorithms. This research was supported in part by the Semiconductor Research Corpora tion, by the National Science Foundation, by Harris Semiconductor, and by the International Business Machines Corporation Resident Study Program. Finally, just for the

record: John Cohn was the designer of the KOAN placer; David Garrod was the designer of the ANAGRAM II router (and its predeces sor, ANAGRAM I). This book was architected by all four authors, edited by John Cohn and Rob Rutenbar, and produced in finished form by John Cohn.

The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology thoroughly examines real-time logic (RTL) to GDSII (a file

format used to transfer data of semiconductor physical layout) design flow, analog/mixed signal design, physical verification, and technology computer-aided design (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability (DFM) at the nanoscale,

power supply network design and analysis, design modeling, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final

phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new

chapters on 3D circuit integration and clock design Offering improved depth and modernity, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Integrated circuits are fundamental electronic components in biomedical, automotive and many other technical systems. A small, yet crucial part of a chip consists of analog circuitry. This part is still in large part designed by hand and therefore represents not only a bottleneck

in the design flow, but also a permanent source of design errors responsible for re-designs, costly in terms of wasted test chips and in terms of lost time-to-market. Layout design is the step of the analog design flow with the least support by commercially available, computer-aided design tools. This book provides a survey

of promising new approaches to automated, analog layout design, which have been described recently and are rapidly being adopted in industry.

The number of gates on a chip is quickly growing toward and beyond the one billion mark. Keeping all the gates running

at the beat of a single or a few rationally related clocks is becoming impossible. In static timing analysis process variations and signal integrity issues stretch the timing margins to the point where they become too conservative and result in significant overdesign. Importance and difficulty of such problems push some

developers to once again turn to asynchronous alternatives. However, the electronics industry for the most part is still reluctant to adopt asynchronous design (with a few notable exceptions) due to a common belief that we still lack a commercial-quality Electronic Design Automation tools (similar to the

synchronous RTL-to-GDSII flow) for asynchronous circuits. The purpose of this paper is to counteract this view by presenting design flows that can tackle large designs without significant changes with respect to synchronous design flow. We are limiting ourselves to four design flows that we believe to be closest to this

goal. We start from the Tangram flow, because it is the most commercially proven and it is one of the oldest from a methodological point of view. The other three flows (Null Convention Logic, de-synchronization, and gate-level pipelining) could be considered together as asynchronous re-implementations of

synchronous (RTL- or gate-level) specifications. The main common idea is substituting the global clocks by local synchronizations. Their most important aspect is to open the possibility to implement large legacy synchronous designs in an almost "push button" manner, where all asynchronous

machinery is hidden, so that synchronous RTL designers do not need to be re-educated. These three flows offer a trade-off from very low overhead, almost synchronous implementations, to very high performance, extremely robust dual-rail pipelines.

This book introduces readers to a variety of tools for analog layout design automation. After discussing the placement and routing problem in electronic design automation (EDA), the authors overview a variety of automatic layout generation tools, as well as the most recent advances in analog layout-aware

circuit sizing. The discussion includes different methods for automatic placement (a template-based Placer and an optimization-based Placer), a fully-automatic Router and an empirical-based Parasitic Extractor. The concepts and algorithms of all the modules are thoroughly described, enabling readers to

reproduce the methodologies, improve the quality of their designs, or use them as starting point for a new tool. All the methods described are applied to practical examples for a 130nm design process, as well as placement and routing benchmark sets.

The explosive growth and development of the integrated circuit market over the last few years have been mostly limited to the digital VLSI domain. The difficulty of automating the design process in the analog domain, the fact that a general analog design methodology remained undefined, and the poor performance of

earlier tools have left the analog

Design Automation: Automated Full-Custom VLSI Layout Using the ULYSSES Design Environment deals with the use of the Ulysses design environment for an automated full-custom VLSI layout. Topics covered include VLSI chip design

and design process, control mechanisms in Ulysses, and the use of artificial intelligence (AI) in design environments. An example design task is also presented. This book is comprised of 10 chapters and begins with an overview of VLSI computer-aided design (CAD), focusing on an expert system based design

environment aimed at solving the CAD tool integration problem. An example CAD tool suite for such an environment is presented. The next chapter describes prior attempts at developing an integrated design environment, followed by a discussion on the computer-aided VLSI design process that motivated the

development of the Ulysses design environment. The following chapters explore the use of AI techniques within Ulysses; the fundamental architecture of Ulysses; and the control mechanisms that govern the decision to execute various CAD tools, on particular files, within Ulysses. The implementation of Ulysses is

also discussed. The final chapter demonstrates the feasibility of a knowledge-based design environment for VLSI chip design applications; the success of Ulysses at further automating the VLSI design process; and the usability of Ulysses as a VLSI design environment. This monograph will be a valuable

resource for systems designers and other practitioners in computer science and computer engineering.

In the first part the AMGIE analog synthesis system is described. AMGIE is the first analog synthesis system that automates the full design process from

specifications down to verified layout. It is targeted to the design of moderate-complexity circuits. It relies on design and circuit knowledge stored in the tool's libraries and can be used by both novice and experienced analog designers as well as system-level designers. The inner workings are explained in detail, with

(practical) examples to demonstrate how the implemented algorithms and techniques work. Experimental results obtained with the AMGIE system are reported, including actual fabricated and measured circuits. The second approach, i.e. the systematic design of high-performance analog circuits, is discussed

in the second part of the book. This approach is supported by tools to boost the productivity of the designer. An example of such a tool is Mondriaan, that is targeted towards the automatic layout generation of highly regular analog blocks. The proposed systematic design methodology is then applied to the design

of high-accuracy current-steering digital to analog converters (DACs). The full design path is discussed in detail. Both complementary approaches increase analog design productivity. Design times of the different design experiments undertaken are reported throughout the book to demonstrate this.

Cell-based design methodologies have dominated layout generation of digital circuits. Unfortunately, the growing demands for transparent process portability, increased performance, and low-level device sizing for timing/power are poorly handled in a fixed cell library.

Direct Transistor-Level Layout For Digital Blocks proposes a direct transistor-level layout approach for small blocks of custom digital logic as an alternative that better accommodates demands for device-level flexibility. This approach captures essential shape-level optimizations, yet scales easily to netlists with thousands of

devices, and incorporates timing optimization during layout. The key idea is early identification of essential diffusion-merged MOS device groups, and their preservation in an uncommitted geometric form until the very end of detailed placement. Roughly speaking, essential groups are extracted early from the

transistor-level netlist, placed globally, optimized locally, and then finally committed each to a specific shape-level form while concurrently optimizing for both density and routability. The essential flaw in prior efforts is an over-reliance on geometric assumptions from large-scale cell-based layout algorithms. Individual

transistors may seem simple, but they do not pack as gates do. Algorithms that ignore these shape-level issues suffer the consequences when thousands of devices are poorly packed. The approach described in this book can pack devices much more densely than a typical cell-based layout. Direct Transistor-Level Layout For Digital

Blocks is a comprehensive reference work on device-level layout optimization, which will be valuable to CAD tool and circuit designers.

Analog integrated circuits are very important as interfaces between the digital parts of integrated electronic systems and

the outside world. A large portion of the effort involved in designing these circuits is spent in the layout phase. Whereas the physical design of digital circuits is automated to a large extent, the layout of analog circuits is still a manual, time-consuming and error-prone task. This is mainly due to the continuous nature of

analog signals, which causes analog circuit performance to be very sensitive to layout parasitics. The parasitic elements associated with interconnect wires cause loading and coupling effects that degrade the frequency behaviour and the noise performance of analog circuits. Device mismatch and thermal effects put a

fundamental limit on the achievable accuracy of circuits. For successful automation of analog layout, advanced place and route tools that can handle these critical parasitics are required. In the past, automatic analog layout tools tried to optimize the layout without quantifying the performance degradation introduced

by layout parasitics. Therefore, it was not guaranteed that the resulting layout met the specifications and one or more layout iterations could be needed. In Analog Layout Generation for Performance and Manufacturability, the authors propose a performance driven layout strategy to overcome this problem. In this

methodology, the layout tools are driven by performance constraints, such that the final layout, with parasitic effects, still satisfies the specifications of the circuit. The performance degradation associated with an intermediate layout solution is evaluated at runtime using predetermined sensitivities. In contrast with other

performance driven layout methodologies, the tools proposed in this book operate directly on the performance constraints, without an intermediate parasitic constraint generation step. This approach makes a complete and sensible trade-off between the different layout alternatives possible at runtime and therefore

eliminates the possible feedback route between constraint derivation, placement and layout extraction. Besides its influence on the performance, layout also has a profound impact on the yield and testability of an analog circuit. In Analog Layout Generation for Performance and Manufacturability, the authors outline a

new criterion to quantify the detectability of a fault and combine this with a yield model to evaluate the testability of an integrated circuit layout. They then integrate this technique with their performance driven routing algorithm to produce layouts that have optimal manufacturability while still meeting their

performance specifications. Analog Layout Generation for Performance and Manufacturability will be of interest to analog engineers, researchers and students.